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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/431,640	11/01/99	HERRELL	D 1001-0062

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EXAMINER	
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ART UNIT	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/431,640	Applicant(s) HERRELL, DENNIS JAMES	
	Examiner Thanh Y. Tran	Art Unit 2841	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____ .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15 and 23-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 November 1999* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2 and 3* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to under 37 CFR 1.83(a) because they fail to show "off-assembly connections" as described in the specification. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). Correction is required.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 10 and 11 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 10, it is unclear as to what Applicant means by "thereby oppose respective of the initial cross-talk signals introduced at a corresponding one of the off-assembly connections by nearest neighbors thereof". The "nearest neighbors" is not defined to any location or area in the electrical assembly.

Regarding claim 11, it is unclear as to what Applicant means by "wherein the array includes a linear array; wherein the nearest neighbors number two; and wherein, for essentially each of the traces, two of the integrated transformer structures (10) are defined there-along to induce respective of the compensating cross-talk signals and thereby oppose respective of the

initial cross-talk signals introduced by the nearest neighbors". Which array is considering a linear array?

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

5. Claims 1-4, 7, 9-12, 14-15, and 23-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Hashim (U.S. 6,107,578).

As to claim 1, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) comprising: traces extending toward respective off-assembly connections (see Figs 1-2, elements T1-T5, R1-R5; col. 2, line 62 - col. 3, line 38); and integrated transformer structures (see Fig. 1, element 10; col. 2, lines 9-38) defined along the traces to induce compensating cross-talk signals having opposing polarity to initial cross-talk signals associated with mutual coupling between adjacent of the off-assembly connections (see Figs. 1-2, col. 2, lines 28-38).

As to claim 2, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein one or more of the integrated transformer structures each comprise: an aperture in a voltage plane (see Figs. 1-2, col. 1, lines 45-60; col. 3, lines 39-55) of the electrical assembly; essentially parallel portions of corresponding pairs of the traces, the essentially

parallel portions passing over the aperture (see Figs. 1-4, elements T1-T5, R1-R5; col. 2, line 63 - col. 3, line 55).

As to claim 3, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein one or more of the integrated transformer structures (10) each comprise: an aperture in a voltage plane of the electrical assembly; and essentially parallel portions of corresponding pairs of the traces, the essentially parallel portions coplanar with the voltage plane and traversing the aperture therein (see Figs. 1-4, col. 1, lines 45-60; col. 3, lines 38-55). [It should be noted: since the voltage is applied to the paths (traces), thus the parallel portions of the paths (traces) coplanar with the voltage plane].

As to claim 4, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) further comprising: the off-assembly connections (see Fig. 1, elements 13).

As to claim 7, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) including a board or card (see Fig. 1, element 14), wherein the off-assembly connections (13) include pins, leads, solder connections or edge connectors; and wherein the traces are formed on the board or card (14) (see Figs. 1-4, elements T1-T5, R1-R5).

As to claim 9, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the traces (see Figs. 1-2, elements T1-T5, R1-R5) and the off-assembly connections (see Fig. 1, elements 13) are on opposing sides of the electrical assembly (see Figs. 1-2); and wherein an electrical connection between a trace (see Figs. 1-2, elements T1-T5, R1-R5) and a respective off-assembly connection (13) includes a plated through hole or conductive via.

As to claim 10, as best understood, figures 1-4 show the electrical assembly (comprising elements 10, 12, 14) wherein the off-assembly connections (13) are organized as an array thereof; and wherein, for each of the traces (Fig. 1, elements T1-T5, R1-R5), one or more of the integrated transformer structures (10) are defined there-along to induce respective of the compensating cross-talk signal and thereby oppose respective of the initial cross-talk signals introduced at a corresponding one of the off-assembly connections (13) by nearest neighbors thereof (see Figs. 1-4, col. 2, lines 28-38).

As to claim 11, as best understood, figures 1-4 show the electrical assembly (comprising elements 10, 12, 14) wherein the array (13) includes a linear array; wherein the nearest neighbors number two; and wherein, for essentially each of the traces (paths), two of the integrated transformer structures (10) are defined there-along to induce respective of the compensating cross-talk signals and thereby oppose respective of the initial cross-talk signals introduced by the nearest neighbors (see Figs. 1-4, col. 2, lines 28-38).

As to claim 12, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the off-assembly connections include one of pins, solder joints, leads, and wires (see Figs. 1-2, col. 2, lines 10-28).

As to claim 14, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the electrical assembly includes a chip carrier (14).

As to claim 15, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the electrical assembly includes a board (14).

As to claim 23, as best understood, claim 23 is similar to claim 1. Thus it is rejected for the same reasons.

As to claim 24, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the electrical traces are respectively coupled to the first and adjacent connections (see Figs. 1-2, elements T1-T5, R1-R5 and 13, col. 2, line 63 - col. 3, line 12).

As to claim 25, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) comprising: traces (see Fig. 2, elements T1-T5, R1-R5) extending toward respective off-assembly connections (see Figs. 1-2, elements 13); and means defined along the traces for inducing compensating cross-talk signals having opposing polarity to initial cross-talk signals associated with mutual coupling between adjacent of the off-assembly connections (see Figs. 1-2, col. 2, lines 28-38).

Claim 26 recites limitations similar to claim 3. Thus it is rejected for the same reasons.

As to claim 27, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the means for inducing compensating cross-talk signals include integrated transformer structures defined along the traces (see Figs. 1-4, elements T1-T5, R1-R5; col. 2, lines 28-38).

As to claim 28, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the means for inducing compensating cross-talk signals define at least a portion of a cross-talk compensation circuit (see Figs. 1-2, col. 2, lines 28-38).

As to claim 29, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) comprising: traces (see Fig. 2, elements T1-T5, R1-R5; col. 2, line 62 - col. 3, line 38) extending toward respective off-assembly connections (Fig. 1, element 13); and essentially parallel portions of the traces traversing apertures (as shown in figures 1-3) defined in one or more voltage planes of the assembly to inductively couple compensating cross-talk signals

having opposing polarity to an original cross-talk signal (see Figs. 1-2, col. 2, lines 28-38; and col. 3, lines 25-55).

As to claim 30, Hashim discloses an electrical assembly (see Fig. 1, comprising elements 10, 12, 14) wherein the aperture traversing portions of the traces (see Figs. 1-2, elements T1-T5, R1-R5) at least partially define integrated, co-planar transformer structures (10) (see Figs. 1-2).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5-6, 8 and 13 rejected under 35 U.S.C. 103(a) as being unpatentable over Hashim (U.S. 6,107,578).

As to claims 5-6, 8 and 13, Hashim does not disclose an electrical assembly including a semiconductor package wherein the off-assembly connections include pins, solder connections, leads, or wires. However, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to have an electrical assembly including a semiconductor package or an integrated circuit chip for the purpose of reducing delay in a semiconductor integrated circuit, improving the noise resistibility, and also reducing the production cost.

Conclusion

8. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Igarashi et al. (U.S. 6,262,487) teaches the Semiconductor Integrated Circuit Device, Semiconductor Integrated Circuit Wiring Method, and Cell Arranging Method.

Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Y. Tran whose telephone number is (703) 305-4757. The examiner can normally be reached on Monday through Thursday and on alternate Fridays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeff Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3431.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

TYT

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